



Packet No.: INTEL-022

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of :
:
Zurab KHASIDASHVILI, John MOONDANOS, and :
Ziyad HANNA : Group Art Unit: 2121
:
Serial No.: 10/608,423 : Examiner: EXAMINER-Unkown
:
Filed: June 30, 2003 : Customer No.: 34610
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For: APPLICATION OF THE RETIMED NORMAL FORM TO THE FORMAL
EQUIVALENCE VERIFICATION OF ABSTRACT RTL DESCRIPTIONS FOR PIPELINED DESIGNS

INFORMATION DISCLOSURE STATEMENT

U.S. Patent and Trademark Office
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Arlington, Virginia 22202

Sir:

Pursuant to 37 C.F.R. 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. One copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the indicated date. Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered. This statement should not be construed as a representation that a search has been made, that information cited in the statement is considered to be and/or is material to patentability, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith. It is further understood that the Examiner will consider information that was cited or submitted to the U.S. Patent and Trademark Office in a prior application relied on under 35 U.S.C. §120. 1138 OG 37, 38 (May 19, 1992).

- X 1. This Information Disclosure Statement is being filed (i) within three months of the U.S. filing date of a U.S. application other than a CPA continued prosecution application under §1.53(d) OR (ii) within three months of the date of entry of the national stage as set forth in §1.491 in an international application OR (iii) before the mailing date of a first Office Action on the merits. No certification or fee is required. 37 C.F.R. §1.97(b).
- 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection OR Notice of Allowance OR an action that otherwise closes prosecution in the application. 37 C.F.R. §1.97(c).

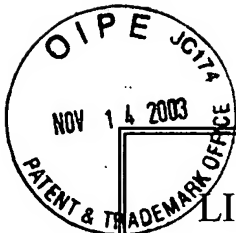
- a. I hereby state that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. 1.97(e)(1).
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- c. Attached is our check no. _____ in the amount of \$180.00 in payment of the fee under 37 C.F.R. 1.17(p). Please credit or debit Deposit Account No. 16-0607 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached.
- 3. This Information Disclosure Statement is being filed after the mailing date of a Final Rejection OR Notice of Allowance OR an action that otherwise closes prosecution in the application, but on or before payment of the Issue Fee. Attached is our check no. ____ in the amount of \$180.00 in payment of the fee under 37 C.F.R. 1.17(p). Please credit or debit Deposit Account No. 16-0607 as needed to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached. 37 C.F.R. §1.97(d).
- a. I hereby state that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. 1.97(e)(1).
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- 4. Others:
- X 5. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 16-0607 and please credit any excess fees to such deposit account.

Respectfully submitted,
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Date: November 14, 2003

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**LIST OF PRIOR ART CITED BY
APPLICANT
(PTO-1449)**

ATTY. DOCKET NO.
INTEL-0022

APPLN. SERIAL NO.
**New U.S. Patent
Application**

APPLICANT(S)
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Ziyad HANNA**

CUSTOMER NO. 34610

FILING DATE
June 30, 2003

GROUP
2121

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	*PATENT NO.	*ISSUE DATE	*INVENTOR NAME	CLASS	SUBCLASS	FILING DATE

U.S. PATENT APPLICATION PUBLICATIONS

	*PATENT APPLN. PUB. NO.	*PUB. DATE	*APPLICANT	CLASS	SUBCLASS	

U.S. PATENT APPLICATIONS

	*APPLN. NO.	*FILING DATE	*INVENTOR	CLASS	SUBCLASS	

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						Yes	No

OTHER ART (Including Author, Title, Date, Pertinent Pages, Publisher, Place of Publication, Etc.)

	Matthew W. Maskewicz, Conor F. Madigan, Ying Zhao, Lintao Zhang, Sharad Malik; Chaff: Engineering an Efficient SAT Solver; June 2001, 530-535; DAC, Las Vegas, Nevada, USA
	R.K Ranjan, V. Singhal, F. Somenzi, and R.K Brayton. Using combinational verification for sequential circuits, in: Proc. of Design, Automation and Test in Europe Conference, DATE'99, 1999.
	Gabriel P. Bischoff, Karl S. Brace, Samir Jain, and Rahul Razdan; Digital equipment Corporation, Digital Semiconductor, 1997, 16-24, IEEE, Hudson, MA 01749
	Rajeev Kumar Ranjan; Design and Implementation Verification of Finite State Systems; Fall 1997; pages 1-330; University of California, Berkeley, California
	Z. Khasidashvili, J. Moondanos, Z. Hanna. TRANS: Efficient Sequential Verification of Loop-Free Circuits. in: Proc. of IEEE International High Level Design Validation and Test Workshop, HLDVT'02, IEEE Computer Society Press, 2002, p. 115-120.

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.